AISG On-Off Keying Coax Modem Transceiver

Check for Samples: SN65HVD62

FEATURES

- **Supply Ranging From 3V to 5.5V**
- **Independent Logic Supply of 1.6V to 5.5V**
- **Wide Input Dynamic Range of –15dBm to +5dBm for Receiver**
- **Power Delivered by the Driver to the Coax can be Adjusted From +3dBm to +6dBm**
- **AISG Compliant Output Emission Profile**
- **Low-power Standby Mode**
- **Direction Control Output for RS-485 Bus Arbitration**
- **Supports up to 115 kbps Signaling**
- **Integrated Active Bandpass Filter in the Receiver Path with Center Frequency at 2.176MHz**
- **3mm × 3mm 16-Pin QFN Package**

APPLICATIONS

- **AISG – Interface for Antenna Line Devices**
- **Tower Mounted Amplifiers (TMA)**
- **General Modem Interfaces**

DESCRIPTION

These transceivers modulate and demodulate signals between the logic (baseband) and a frequency suitable for long coaxial media.

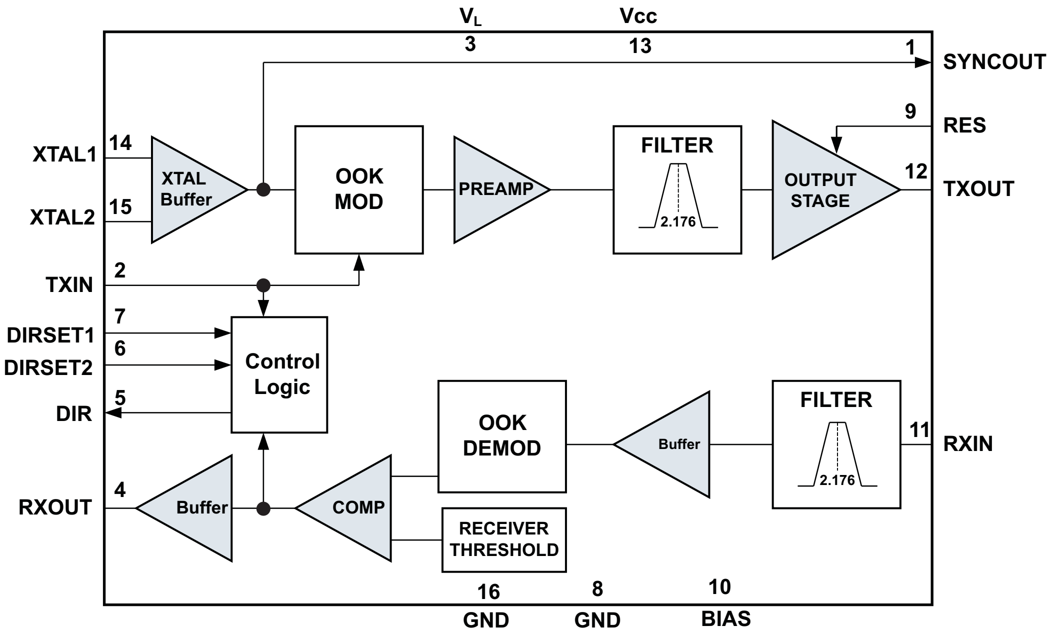
The HVD62 is an integrated AISG transceiver designed to be compliant with Antenna Interface Standards Group v2.0 specification.

The HVD62 receiver integrates an active bandpass filter to enable demodulation of signals even in the presence of spurious frequency components. The filter has a 2.176 MHz center frequency.

The transmitter supports adjustable output power levels varying from +3dBm to +6dBm delivered to the 50 Ω coax cable. The HVD62 transmitter is compliant with the spectrum emission requirement provided by the AISG standard.

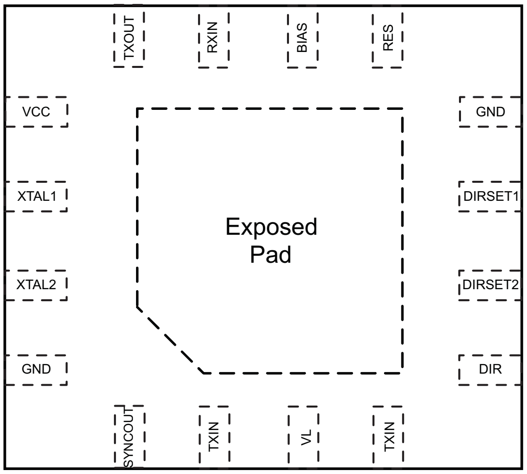
A direction control output is provided which facilitates bus arbitration for an RS-485 interface. These devices integrate an oscillator input for a crystal, and also accept standard clock inputs to the oscillator.

PRODUCT PREVIEW



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN CONFIGURATION



PIN FUNCTIONS

PIN	HVD62 PIN	DESCRIPTION
	NAME	
1	SYNCOUT	Open drain output to synchronise other devices to the 4x-carrier oscillator at XTAL1,2. (8.704 MHz for HVD62)
2	TXIN	Digital data bit stream to driver.
3	VL	Logic supply voltage for the device.
4	RXOUT	Digital data bit stream from receiver.
5	DIR	DIR: Direction control output signal for bus arbitration. DIRSET, DIRSET1 and DIRSET2: Bits to set the duration of DIR DIRSET[2,1]:[L,L]=9.6kbps [L,H]=38.4kbps [H,L]=115kbps [H,H]=Standby Mode
6	DIRSET2	
7	DIRSET1	
8	GND	Ground
9	RES	Resistor used to adjust driver output power.
10	BIAS	Bias setting resistor.
11	RXIN	Modulated input signal to the receiver.
12	TXOUT	Modulated output signal from the driver.
13	VCC	Analog supply voltage for the device.
14	XTAL1	Crystal oscillator’s IO pins. Connect a 4 x f_C crystal between these pins. Or connect XTAL1 to an 8.704 MHz clock and connect XTAL2 to GND.
15	XTAL2	
16	GND	Ground
-	EP	Exposed pad. To be connected electrically to GND.

ABSOLUTE MAXIMUM RATINGS(1)

	VALUES
Supply voltage, V_{CC} and V_L	–0.5 V to 6 V
Voltage range at coax pins	–0.5 V to 6 V
Voltage range at logic pins	–0.3 V to V_L + 0.3 V
Electrostatic Discharge, Human Body Model (EIA/JESD 22-A114)	±2 kV
Logic Output Current	–20 mA to 20 mA
TXOUT output current	Internally limited
SYNCOUT output current	Internally limited
Junction Temperature, T_J	170°C
Continuous total power dissipation	See Thermal Table

(1) † Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		SN65HVD62 QFN (16) PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance		°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance		
θ_{JB}	Junction-to-board thermal resistance		
ψ_{JT}	Junction-to-top characterization parameter		
ψ_{JB}	Junction-to-board characterization parameter		
θ_{JCbot}	Junction-to-case (bottom) thermal resistance		

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Analog supply voltage		3		5.5	V
V_L	Logic supply voltage		1.6		5.5	V
$V_{I(pp)}$	Input signal amplitude at RXIN				1.12	Vpp
V_{IH}	High-level input voltage	TXIN, DIRSET1, DIRSET2	70%V_L		V_L	V
		XTAL1, XTAL2	70%V_{CC}		V_{CC}	
V_{IL}	Low-level input voltage	TXIN, DIRSET1, DIRSET2	0		30%V_L	V
		XTAL1, XTAL2	0		30%V_{CC}	
$1/t_{UI}$	Data signaling rate		9.6		115	kbps
F_{OSC}	Oscillator frequency	HVD62	–30 ppm	8.704	30 ppm	MHz
T_A	Operating free-air temperature		–40		85	°C
T_J	Junction Temperature		–40		125	°C
R_{LOAD}	Load impedance between TXOUT to RXIN			50		Ω
	Load impedance between RXIN and GND at f_C (channel)			50		
R1	Bias resistor between BIAS and RES			4.1		kΩ
R2	Bias resistor between RES and GND			10		kΩ
R_{SYNC}	Pull-up resistor between SYNCOUT and V_{CC}			1		kΩ
V_{RES}	Voltage at RES pin		0.84		1.5	V
C_C	Coupling capacitance between RXIN and Coax (channel)			270		nF
C_{BIAS}	Capacitance between BIAS and GND			1		μF

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY								
100	I_{CC}	Supply current (V_{CC})	TXIN = L (Active)	DIRSET1 = L DIRSET2 = H		26.5	33	mA
101			TXIN = H (Quiescent)			25	30	
102			TXIN = 115kbps, 50% duty cycle			27	33	
99			(Standby) DIRSET1=DIRSET2=H			12	17	
103	I_L	Logic supply current	TXIN = H, RXIN = DC input				300	μA
104	$\Delta V_{RXIN}/\Delta V_{CC}$	Receiver power supply rejection ratio	$V_{TXIN} = V_L$		49	60		dB
105	$\Delta V_{TXOUT}/\Delta V_{CC}$	Driver power supply rejection ratio	V_{TXIN} = 0 V		49	60		dB
LOGIC PINS								
112	V_{OH}	High-level logic output voltage (RXOUT, DIR)	I_{OH} = –4 mA		90%V_L			V
113	V_{OL}	Low-level logic output voltage (RXOUT, DIR)	I_{OL} = 4 mA				10%V_L	V
114	I_{IH}/I_{IL}	Logic input current (TXIN, DIRSET1/2)	Shorted to GND or VL				±1	μA
122	I_{IH_XTAL}/I_{IL_XTAL}	Input current for XTALI/XTALO pins			TBD		TBD	μA
COAX DRIVER								
130	V_{OPP}	Peak-to-peak output voltage at device pin TXOUT (See Figure 1)	V_{RES} = 1.5 V (Maximum setting)		2.24	2.5		V_{PP}
132			V_{RES} = 0.7 V (Minimum setting)			1.17	1.3	
130A	V_{OPP}	Peak-to-peak voltage at coax out (See Figure 1)	V_{RES} = 1.5 V		5	6	6.9	dBm
132A			V_{RES} = 0.7 V		–1.6	-0.6	0.3	
134	V_{OZ}	Off-state output voltage	At TXOUT				5	mVpp
134A			At coax out				-40	dBm
136		Output emissions TBD dBm at f_C = 2.176 MHz	f ≤ 1 MHz				–41	dBm
137			f = f_O ± 200 kHz				–10	dBm
138			f = f_O ± 500 kHz				–30	dBm
139			10 MHz < f < 25 MHz				–41	dBm
140			25 MHz < f (1)				–72	dBm
141	fo	Output frequency (HVD62)				2.176		MHz
142	Δf	Output frequency variation			–100		100	ppm
143	Zo	Output impedance	At DC			0.03		Ω
144			At 10MHz			2.5		Ω
145	I_{OS}	Short-circuit output current			–200		200	mA
COAX RECEIVER								
152	V_{IT}	Input threshold	f_{IN} = 2.176 MHz		79	112	158	mVPP
152A					–18	–15	–12	dBm
154	Z_{IN}	Input impedance	f = f_O		11	27		kΩ
RECEIVER FILTER (HVD62)								
160	f_{PB}	Passband	VRXIN = 1.12VP_P		1.1		4.17	MHz
161	f_{REJ}	Receiver rejection range	2.176MHz carrier amplitude of 112.4 mV_{PP}, Frequency band of spurious components with 800 mVPP allowed.		1.1		4.17	MHz
XTAL AND SYNC								
171	I_I	Input leakage current	XTAL1, XTAL2, 0V < VIN < Vcc		–10		10	μA
172	V_{OL}	Output low voltage	SYNCOUT, with 1 kΩ resistor from SYNCOUT to Vcc				0.4	V

(1) Specified by design with a recommended 470 pF capacitor between RXIN and GND. Measurements above 150 MHz are determined by setup

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
201	t_{pAQ}, t_{pQA}	Coax driver propagation delay	See Figure 1			5	μs
202	t_r, t_f	Coax receiver output rise/fall time	C_L = 15 pF, R_L = 1 kΩ, See Figure 1		20		ns
203	t_{PHL}, t_{PLH}	Receiver propagation delay	See Figure 2		5.5	11	μs
204	DC	Coax receiver output duty cycle	V_{RXIN} = 630 mVpp (0 dBm) with 50% duty cycle	40%		60%	
214			V_{RXIN} = 200 mVpp (–10 dBm) with 50% duty cycle	40%		60%	
206	t_{DIR}	Direction control active duration	DIRSET2 = DIRSET1 = GND or OPEN		1667		μs
207			DIRSET2=GND, DIRSET1=VL		417		
208			DIRSET2=VL, DIRSET1=VL		137		
209	$t_{DIR\ Skew}$	Direction control skew (DIR to RXOUT)		270			ns

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

Signal generator rate is 115 kbps, 50% duty cycle, rise and fall times less than 6 nsec, nominal output levels 0V and 3V. Coupling capacitor Cc is 270 nF.

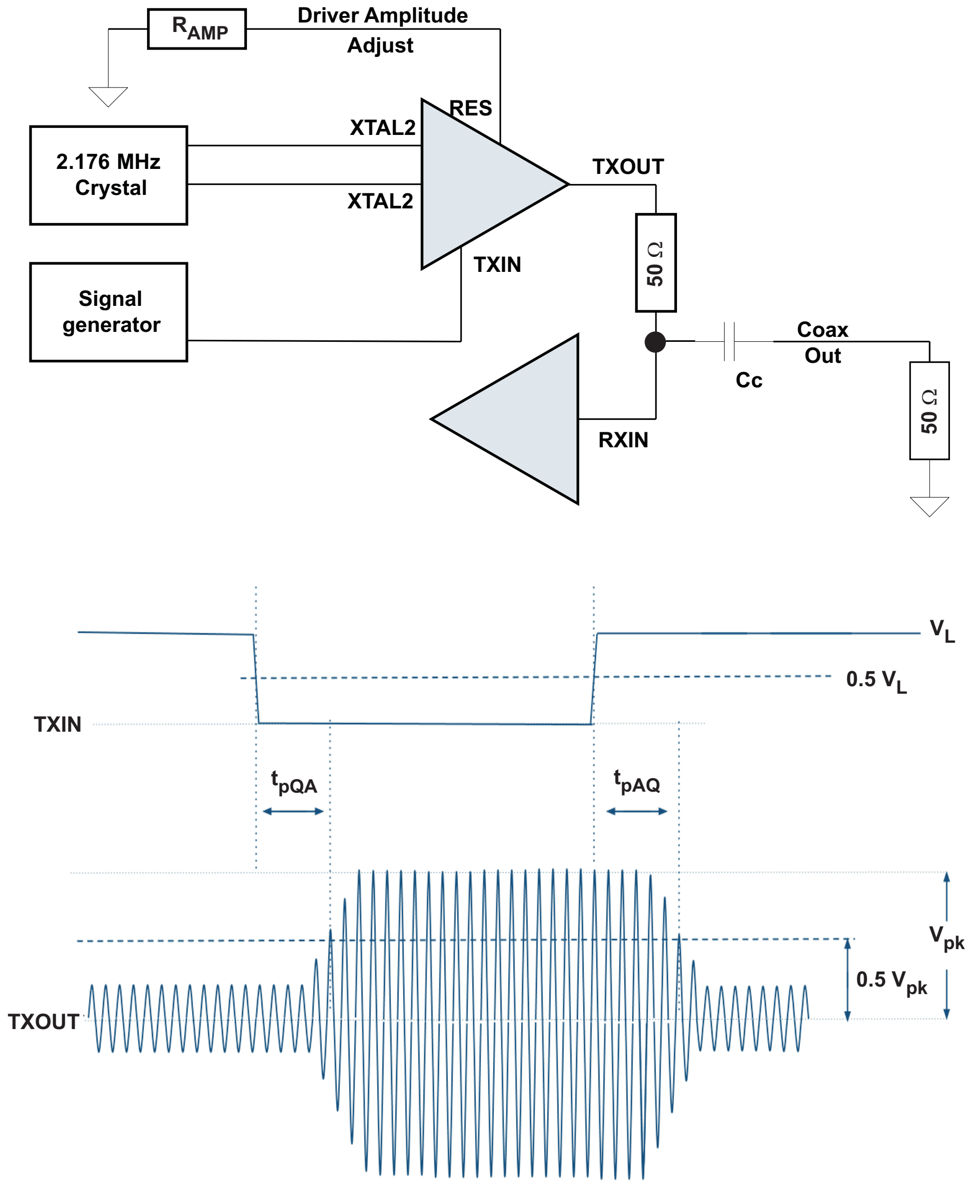


Figure 1. Measurement of Modem Driver Output Voltage With 50 Ω Loads

PARAMETER MEASUREMENT INFORMATION (continued)

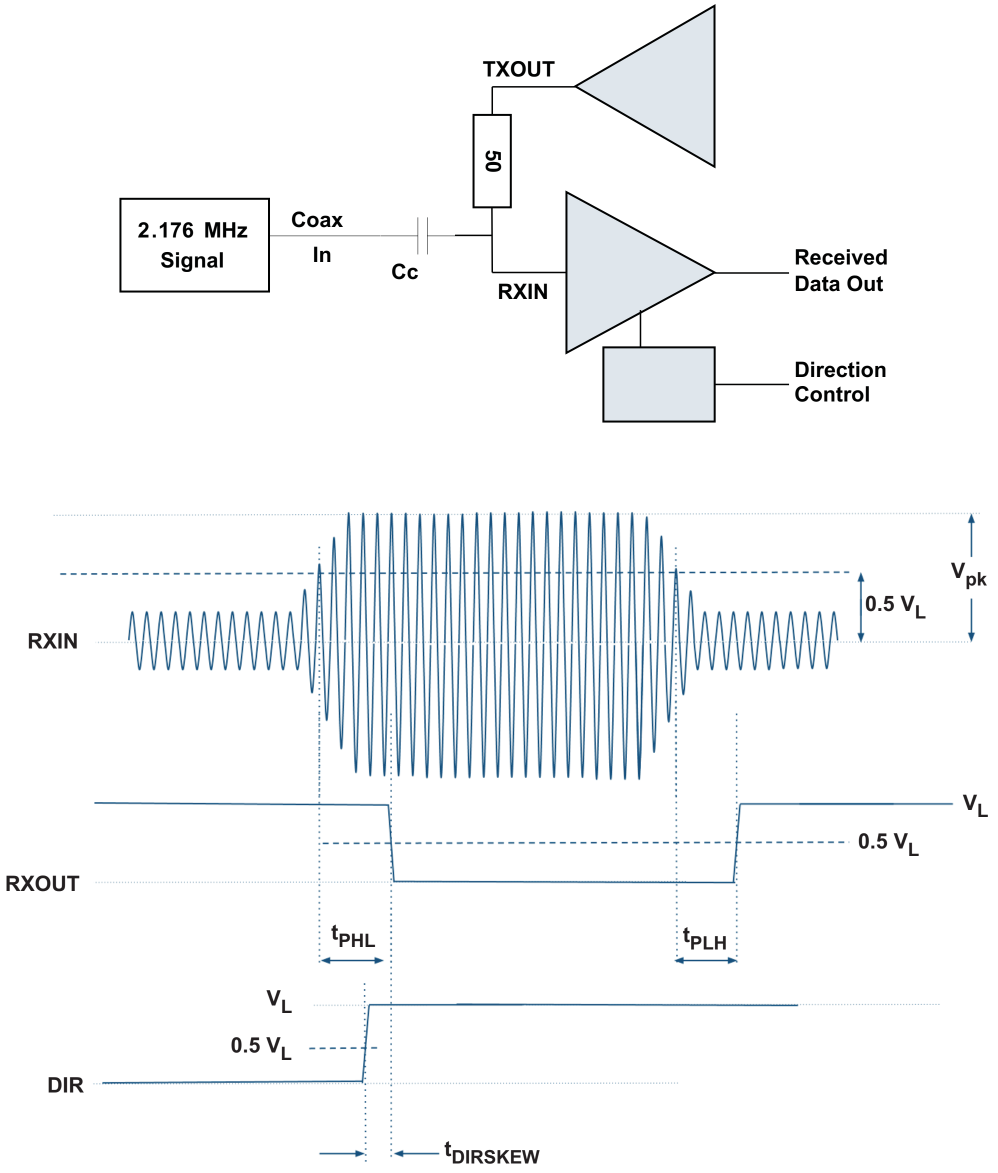


Figure 2. Measurement of Modem Receiver Propagation Delays

TYPICAL CHARACTERISTICS

Figure 3. Emissions Spectrum near f_c = 10 MHz

Figure 4. Emissions Spectrum above f_c = 10 MHz

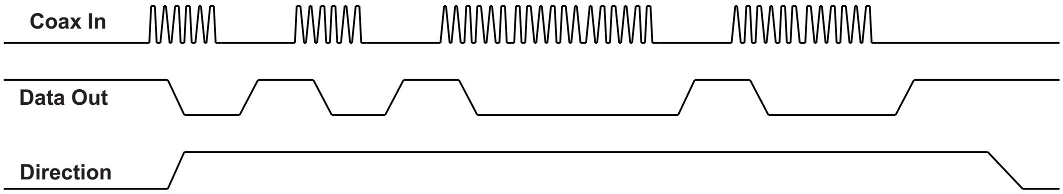
DEVICE APPLICATION INFORMATION

Driver Amplitude Adjust

External resistors are used to set the amplitude of the modulated driver output signal. Resistors connected across RSET and RBIAS together set the output power delivered.

Direction Control

In many applications the mast-top modem which receives data from the base will then distribute the received data through an RS-485 network to several mast-top devices. When the mast-top modem receives the first logic 0 bit (active modulated signal) it will take control of the mast-top RS-485 network by asserting the Direction Control signal. The duration of the Duration Control assertion should be optimized to pass a complete message of length B bits at the known signaling rate (1/tBIT) before relinquishing control of the mast-top RS-485 network. For example, if the messages are 10 bits in length (B=10) and the signaling rate is 9600 bits per second (tBIT = 0.104 msec) then a positive pulse of duration 2 msec would enable the mast-top RS-485 drivers to distribute each received message.



DIRECTION Control Time Constant

The time constant for the Direction Control function can be set by the Control Mode pins, DIRSET1/DIRSET2. These pins should be set to correspond to the desired data rate. With no external connections to the Control Mode pins, the internal time constant is set to the maximum value, corresponding to the minimum data rate.

Conversion Between dBm and Peak-to-peak Voltage

dBm = 20 × LOG10 [Volts-pp / SQRT(0.008 × Z_o)] = 20 × LOG10 [Volts-pp / 0.63] for Z_o = 50 Ω
Volts-pp = SQRT(0.008 × Z_o) × 10^(dBm/20) = 0.63 × 10^(dBm/20) for Z_o = 50 Ω

The following table shows conversions between dBm and peak-to-peak voltage with 50 Ohm load, for various levels of interest including reference levels from the 3GPP TS 25.461 Technical Specification.

Signal on Coax (Iuant Layer 1)	dBm	Vpp (V)
Maximum Driver ON Signal	5	1.12
Nominal Driver ON Signal	3	0.89
Minimum Driver ON Signal	1	0.71
AISG Maximum Receiver Threshold	–12	0.16
Nominal Receiver Threshold	–15	0.11
Minimum Receiver Threshold	–18	0.08
Maximum Driver OFF Signal	–40	0.006

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SN65HVD62RGT	PREVIEW	QFN	RGT	16	250	TBD	Call TI	Call TI	
SN65HVD62RGTR	PREVIEW	QFN	RGT	16	3000	TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
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OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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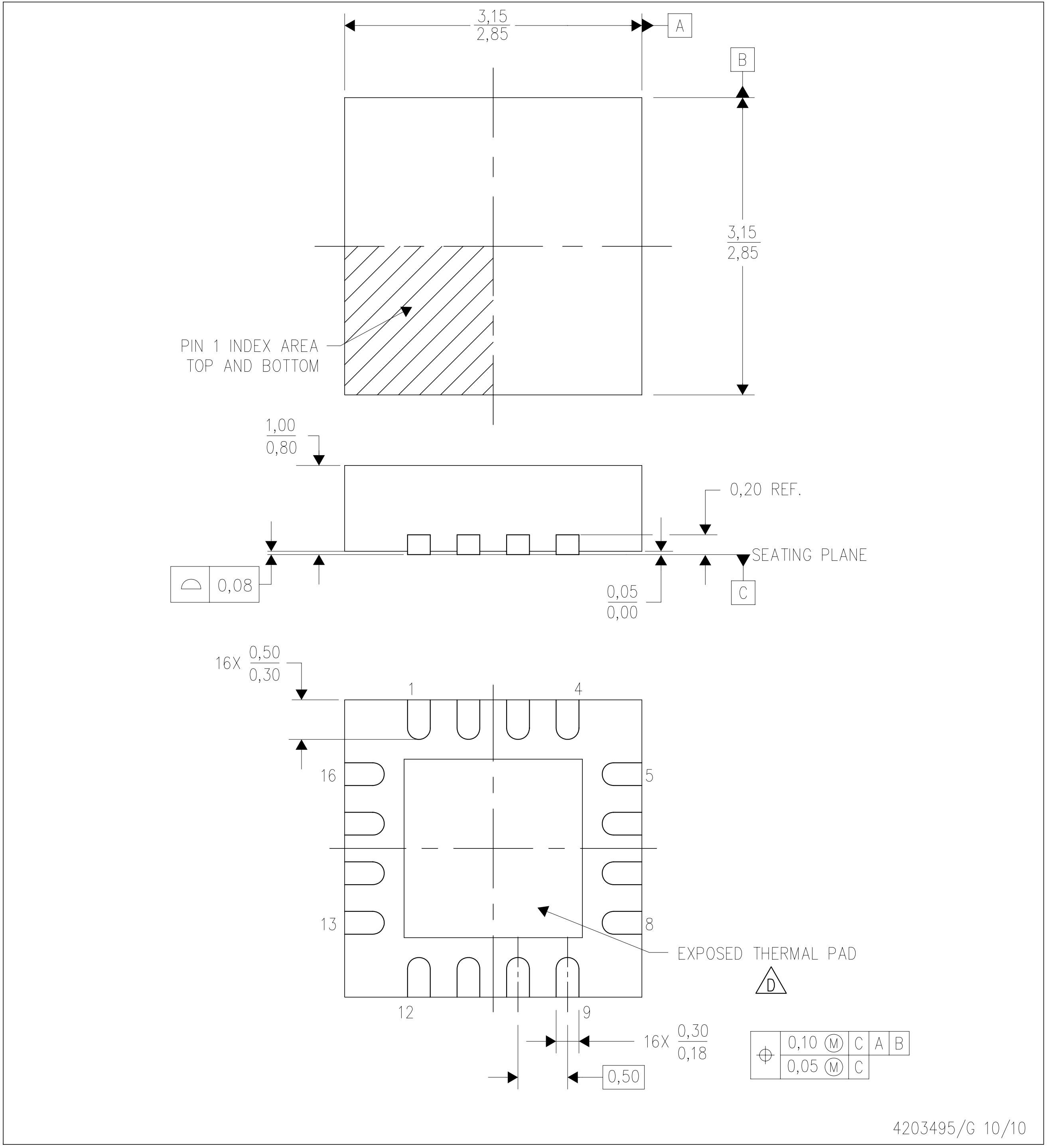
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No–leads (QFN) package configuration.
- △D The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MO–220.

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